

## FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

Applicant(s): D.E. Parson et al.  
 Case: 3-2-1-4  
 Serial No.: 09/583,057  
 Filing Date: May 30, 2000  
 Group: TBA

2763

## U.S. PATENT DOCUMENTS

EXAMINER				FILING DATE	
INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

EXAMINER				TRANSLATION	
INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	YES NO

## OTHER DOCUMENTS

EXAMINER		
INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

- TB 1. D. Jaskolski, "How to Design an IDE for Debugging Multi-processor DSP Systems," Engineering, pp. 1-17, June 2000.
- TB 2. Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1, "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE, New York, NY, October 1993.
- TB 3. Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1b, "Supplement to IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE, New York, NY, March 1995.

RECEIVED  
 SEP 28 2000  
 TECH CENTER 2760

Examiner

Date Considered

2/24/03

**Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

## FORM PTO-1449 (MODIFIED)

Applicant(s): D.E. Parson et al.  
 Case: 3-2-1-4  
 Serial No.: TBA  
 Filing Date: May 30, 2000  
 Group: TBA

LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

JC835 U.S. PTO  
 09/583057  
 05/30/00

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
---------------------	--------------	------	------	----------------	-------------------------------

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES NO
---------------------	--------------	------	---------	----------------	-----------------------

## OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
---------------------	---------	--

- TB 1. L. Goudge, "Debugging Embedded Systems," ARM White Paper, www.arm.com, 6 pages, 1998.
- TB 2. ScanProgrammer Product Information, ASSET InterTech, www.asset-intertech.com, 37 pages, March 2000.
- TB 3. Advanced Tutorial: Using the MVP Multiprocessing Features, Chapter 3, www.ti.com, pp. 3-1 through 3-17, undated.
- TB 4. Using the Parallel Debug Manager, Chapter 11, www.ti.com, pp. 11-1 through 11-21, undated.
- TB 5. BDM/JTAG Debug Interfaces, http://www.abatronag.ch, 6 pages, February 2000.
- TB 6. Multi-ICE™ Interface Unit, wysiwyg://4/http://www.arm.com, pp. 1-4, 2000.
- TB 7. Summit-ICE PCI Emulator, http://www.wmdsp.com, 1 page, 1998.
- TB 8. Mountain-ICE/WS JTAG Emulator-SBus, http://www.wmdsp.com, pp. 1-2, 1998.
- TB 9. Mountain-ICE JTAG Emulator-PC-ISA, http://www.wmdsp.com, pp. 1-2, 1998.

Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.